

UNITED STATES PATENT AND TRADEMARK OFFICE  
**CERTIFICATE OF CORRECTION**

PATENT NO. : 7,103,041 B1  
APPLICATION NO. : 09/610116  
DATED : September 5, 2006  
INVENTOR(S) : Speiser et al.

Page 1 of 19

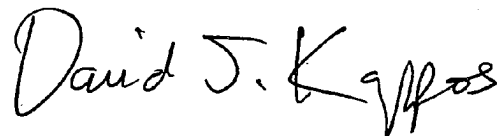
It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Under Columns 21-56, delete handwritten numbers “41”, “42”, “43”, “44”, “45”, “46”, “47”, “48”, “49”, “50”, “51”, “52”, “53”, “54”, “55”, “56”, “57”, “58”.

In Column 26, below Figure, Line 2, delete “disab” and insert -- disabled) --, therefor.

Signed and Sealed this

Twenty-sixth Day of January, 2010

A handwritten signature in black ink that reads "David J. Kappos". The signature is written in a cursive, flowing style.

David J. Kappos  
*Director of the United States Patent and Trademark Office*

**APPENDIX**

BFS Backplane Optimization Worksheet

Notes:

1) Colors are used to represent the use/reuse of serial communication channels.

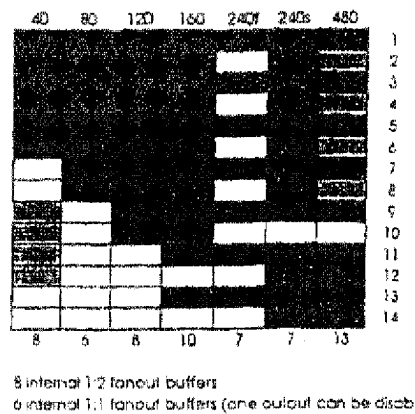


idle  
committed  
used in next config (off limits for this config)  
2nd use of receiver/transmitter  
3rd use of receiver/transmitter

2) Channel assignments are optimized for multiple variables:

- Minimization of I/O. Quad GE transceivers provide 1:2 fanout buffers and 2:1 multiplexers. 1:3 fanout or 3:1 fanin requires additional external devices.
- Partitioning of PCB routing complexity. The ASIC to quad GE buses are ideally straight and interleaved (striper with unsnipper and aggregator with separator) to simplify the routing of these clocked buses. The serial connections from quad GE transceivers to core edge connector on fabric and blocks require significant untangling (with minimal use of vias) to group signals by common destination on the edge connector. This is required to reduce the complexity of the backplane routing and corresponding layer count.
- Maximization of symmetry between ASIC's. This symmetry allows interleaving of buses and reduces the need for external mux's and fanout buffers. It may also reduce the complexity of ASICs by reducing the number of unique mux/demux structures. Consequently, the striper map is a subset of the unsnipper map, and both aggregator maps and the separator 5:8 map are derived from the separator 1:4 map.

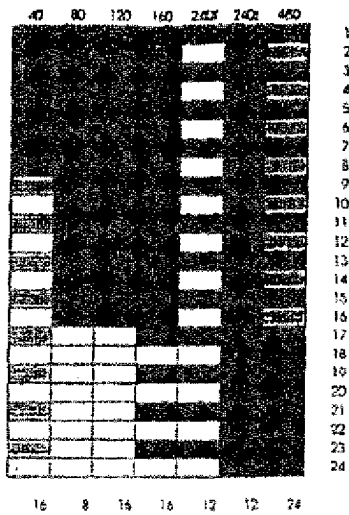
Striper		8	6	8	10	7	7	13
# active tx		10		10		7		13
# fabrics		1	2	3	4	6	6	12
configuration		40	80	120	160	240f	240s	480
S_1A1		1	1	1	1	1	1	1
S_1A2		2	2	2	2			
S_1A3		11						
S_1A4		9						
F1_1A1		3	3	3	3	3	3	3
F1_1A2		4	4	4	4			
F1_1A3		12						
F1_1A4		10						
F2_1A1		5	5	5	5	5	5	5
F2_1A2		6	6	6				
F3_1A1		7	7	7	7	7		
F3_1A2		8	8					
F4_1A1		9	9	9	9			
F4_1A2		10						
F5_1A1		11	11	11	11			
F6_1A1		13	13	13				
F7_1A1					2			
F8_1A1					4			
F9_1A1					6			
F10_1A1					8			
F11_1A1					12			
F12_1A1					14			
Total		22						



		Addresser 1-4								
Receiver 11		16	8	16	16	17	12	24		
F160B1		16 16 16 16 16 16 16 16								
F160B2		16 16 16 16 16 16 16 16								
F160B3		16 16 16 16 16 16 16 16								
F160B4		16 16 16 16 16 16 16 16								
F160B5		16 16 16 16 16 16 16 16								
F160B6		16 16 16 16 16 16 16 16								
F160B7		16 16 16 16 16 16 16 16								
F160B8		16 16 16 16 16 16 16 16								
F160B9		16 16 16 16 16 16 16 16								
F160B10		16 16 16 16 16 16 16 16								
F160B11		16 16 16 16 16 16 16 16								
F160B12		16 16 16 16 16 16 16 16								
F160B13		16 16 16 16 16 16 16 16								
F160B14		16 16 16 16 16 16 16 16								
F160B15		16 16 16 16 16 16 16 16								
F160B16		16 16 16 16 16 16 16 16								
F160B17		16 16 16 16 16 16 16 16								
F160B18		16 16 16 16 16 16 16 16								
F160B19		16 16 16 16 16 16 16 16								
F160B20		16 16 16 16 16 16 16 16								
F160B21		16 16 16 16 16 16 16 16								
F160B22		16 16 16 16 16 16 16 16								
F160B23		16 16 16 16 16 16 16 16								
F160B24		16 16 16 16 16 16 16 16								
F160B25		16 16 16 16 16 16 16 16								
F160B26		16 16 16 16 16 16 16 16								
F160B27		16 16 16 16 16 16 16 16								
F160B28		16 16 16 16 16 16 16 16								
F160B29		16 16 16 16 16 16 16 16								
F160B30		16 16 16 16 16 16 16 16								
F160B31		16 16 16 16 16 16 16 16								
F160B32		16 16 16 16 16 16 16 16								
F160B33		16 16 16 16 16 16 16 16								
F160B34		16 16 16 16 16 16 16 16								
F160B35		16 16 16 16 16 16 16 16								
F160B36		16 16 16 16 16 16 16 16								
F160B37		16 16 16 16 16 16 16 16								
F160B38		16 16 16 16 16 16 16 16								
F160B39		16 16 16 16 16 16 16 16								
F160B40		16 16 16 16 16 16 16 16								
F160B41		16 16 16 16 16 16 16 16								
F160B42		16 16 16 16 16 16 16 16								
F160B43		16 16 16 16 16 16 16 16								
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F160B45		16 16 16 16 16 16 16 16								
F160B46		16 16 16 16 16 16 16 16								
F160B47		16 16 16 16 16 16 16 16								
F160B48		16 16 16 16 16 16 16 16								
F160B49		16 16 16 16 16 16 16 16								
F160B50		16 16 16 16 16 16 16 16								
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F160B54		16 16 16 16 16 16 16 16								
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F160B58		16 16 16 16 16 16 16 16								
F160B59		16 16 16 16 16 16 16 16								
F160B60		16 16 16 16 16 16 16 16								
F160B61		16 16 16 16 16 16 16 16								
F160B62		16 16 16 16 16 16 16 16								
F160B63		16 16 16 16 16 16 16 16								
F160B64		16 16 16 16 16 16 16 16								
F160B65		16 16 16 16 16 16 16 16								
F160B66		16 16 16 16 16 16 16 16								
F160B67		16 16 16 16 16 16 16 16								
F160B68		16 16 16 16 16 16 16 16								
F160B69		16 16 16 16 16 16 16 16								
F160B70		16 16 16 16 16 16 16 16								
F160B71		16 16 16 16 16 16 16 16								
F160B72		16 16 16 16 16 16 16 16								
F160B73		16 16 16 16 16 16 16 16								
F160B74		16 16 16 16 16 16 16 16								
F160B75		16 16 16 16 16 16 16 16								
F160B76		16 16 16 16 16 16 16 16								
F160B77		16 16 16 16 16 16 16 16								
F160B78		16 16 16 16 16 16 16 16								
F160B79		16 16 16 16 16 16 16 16								
F160B80		16 16 16 16 16 16 16 16								
F160B81		16 16 16 16 16 16 16 16								
F160B82		16 16 16 16 16 16 16 16								
F160B83		16 16 16 16 16 16 16 16								
F160B84		16 16 16 16 16 16 16 16								
F160B85		16 16 16 16 16 16 16 16								
F160B86		16 16 16 16 16 16 16 16								
F160B87		16 16 16 16 16 16 16 16								
F160B88		16 16 16 16 16 16 16 16								
F160B89		16 16 16 16 16 16 16 16								
F160B90		16 16 16 16 16 16 16 16								
F160B91		16 16 16 16 16 16 16 16								
F160B92		16 16 16 16 16 16 16 16								
F160B93		16 16 16 16 16 16 16 16								
F160B94		16 16 16 16 16 16 16 16								
F160B95		16 16 16 16 16 16 16 16								
F160B96		16 16 16 16 16 16 16 16								
F160B97		16 16 16 16 16 16 16 16								
F160B98		16 16 16 16 16 16 16 16								
F160B99		16 16 16 16 16 16 16 16								
F160B100		16 16 16 16 16 16 16 16								

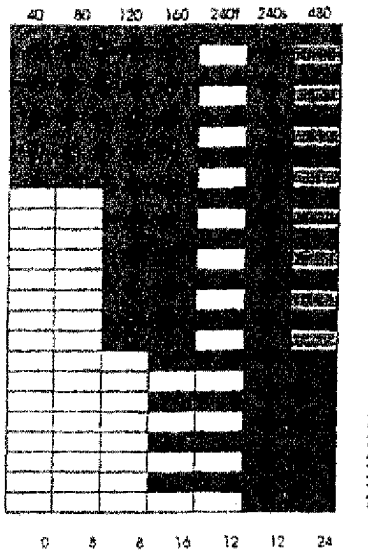
increments by 8

40 total



8 internal: 1:1 button (one input can be turned off)

		Approx. 5-8									
Active rx		0	8	16	24	32	40	48	56		
Stations		1	2	3	4	5	6	7	8		
Configuration		40	80	120	160	240	320	400	480		
F1_5A1	5A	1	1	1	1	1	1	1	1	1	1
F1_5A2	5A	2	2	2	2	2	2	2	2	2	2
F1_5B1	5B	3	3	3	3	3	3	3	3	3	3
F1_5B2	5B	4	4	4	4	4	4	4	4	4	4
F1_5C1	5C	5	5	5	5	5	5	5	5	5	5
F1_5C2	5C	6	6	6	6	6	6	6	6	6	6
F1_5D1	5D	7	7	7	7	7	7	7	7	7	7
F1_5D2	5D	8	8	8	8	8	8	8	8	8	8
F1_13A1	13A	9	9	9	9	9	9	9	9	9	9
F1_13A2	13A	10	10	10	10	10	10	10	10	10	10
F1_13B1	13B	11	11	11	11	11	11	11	11	11	11
F1_13B2	13B	12	12	12	12	12	12	12	12	12	12
F1_13C1	13C	13	13	13	13	13	13	13	13	13	13
F1_13C2	13C	14	14	14	14	14	14	14	14	14	14
F1_13D1	13D	15	15	15	15	15	15	15	15	15	15
F1_13D2	13D	16	16	16	16	16	16	16	16	16	16
F1_21A1	21A	17	17	17	17	17	17	17	17	17	17
F1_21B1	21B	18	18	18	18	18	18	18	18	18	18
F1_21C1	21C	19	19	19	19	19	19	19	19	19	19
F1_21D1	21D	20	20	20	20	20	20	20	20	20	20
F1_29A1	29A	21	21	21	21	21	21	21	21	21	21
F1_29B1	29B	22	22	22	22	22	22	22	22	22	22
F1_29C1	29C	23	23	23	23	23	23	23	23	23	23
F1_29D1	29D	24	24	24	24	24	24	24	24	24	24
F1_37A1	37A	25	25	25	25	25	25	25	25	25	25
F1_37B1	37B	26	26	26	26	26	26	26	26	26	26
F1_37C1	37C	27	27	27	27	27	27	27	27	27	27
F1_37D1	37D	28	28	28	28	28	28	28	28	28	28
F1_45A1	45A	29	29	29	29	29	29	29	29	29	29
F1_45B1	45B	30	30	30	30	30	30	30	30	30	30
F1_45C1	45C	31	31	31	31	31	31	31	31	31	31
F1_45D1	45D	32	32	32	32	32	32	32	32	32	32

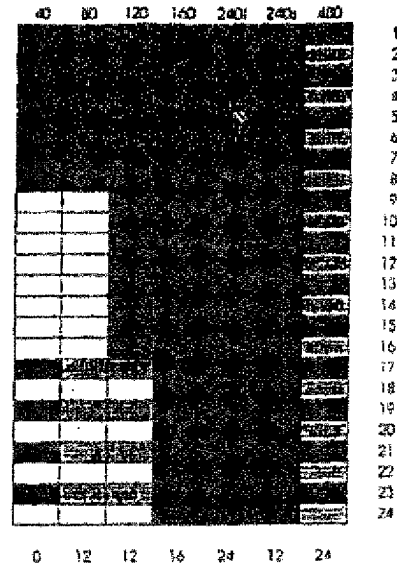


Internal 2:1 Mux's  
16 internal 1:1 buffers (one input can be turned off)

Separator 1-4									
Port	1	2	3	4	5	6	7	8	9
1	20	12	16	16	24	10	24		
2		20	24	24	24	24	24		
3	1	2	3	4	5	6	7	8	9
4	10	10	10	10	10	10	10	10	10
5	1	2	3	4	5	6	7	8	9
6	1	2	3	4	5	6	7	8	9
7	1	2	3	4	5	6	7	8	9
8	1	2	3	4	5	6	7	8	9
9	1	2	3	4	5	6	7	8	9
10	1	2	3	4	5	6	7	8	9
11	1	2	3	4	5	6	7	8	9
12	1	2	3	4	5	6	7	8	9
13	1	2	3	4	5	6	7	8	9
14	1	2	3	4	5	6	7	8	9
15	1	2	3	4	5	6	7	8	9
16	1	2	3	4	5	6	7	8	9
17	1	2	3	4	5	6	7	8	9
18	1	2	3	4	5	6	7	8	9
19	1	2	3	4	5	6	7	8	9
20	1	2	3	4	5	6	7	8	9
21	1	2	3	4	5	6	7	8	9
22	1	2	3	4	5	6	7	8	9
23	1	2	3	4	5	6	7	8	9
24	1	2	3	4	5	6	7	8	9
25	1	2	3	4	5	6	7	8	9
26	1	2	3	4	5	6	7	8	9
27	1	2	3	4	5	6	7	8	9
28	1	2	3	4	5	6	7	8	9
29	1	2	3	4	5	6	7	8	9
30	1	2	3	4	5	6	7	8	9
31	1	2	3	4	5	6	7	8	9
32	1	2	3	4	5	6	7	8	9
33	1	2	3	4	5	6	7	8	9
34	1	2	3	4	5	6	7	8	9
35	1	2	3	4	5	6	7	8	9
36	1	2	3	4	5	6	7	8	9
37	1	2	3	4	5	6	7	8	9
38	1	2	3	4	5	6	7	8	9
39	1	2	3	4	5	6	7	8	9
40	1	2	3	4	5	6	7	8	9
41	1	2	3	4	5	6	7	8	9
42	1	2	3	4	5	6	7	8	9
43	1	2	3	4	5	6	7	8	9
44	1	2	3	4	5	6	7	8	9
45	1	2	3	4	5	6	7	8	9
46	1	2	3	4	5	6	7	8	9
47	1	2	3	4	5	6	7	8	9
48	1	2	3	4	5	6	7	8	9
49	1	2	3	4	5	6	7	8	9
50	1	2	3	4	5	6	7	8	9
51	1	2	3	4	5	6	7	8	9
52	1	2	3	4	5	6	7	8	9
53	1	2	3	4	5	6	7	8	9
54	1	2	3	4	5	6	7	8	9
55	1	2	3	4	5	6	7	8	9
56	1	2	3	4	5	6	7	8	9
57	1	2	3	4	5	6	7	8	9
58	1	2	3	4	5	6	7	8	9
59	1	2	3	4	5	6	7	8	9
60	1	2	3	4	5	6	7	8	9
61	1	2	3	4	5	6	7	8	9
62	1	2	3	4	5	6	7	8	9
63	1	2	3	4	5	6	7	8	9
64	1	2	3	4	5	6	7	8	9
65	1	2	3	4	5	6	7	8	9
66	1	2	3	4	5	6	7	8	9
67	1	2	3	4	5	6	7	8	9
68	1	2	3	4	5	6	7	8	9
69	1	2	3	4	5	6	7	8	9
70	1	2	3	4	5	6	7	8	9
71	1	2	3	4	5	6	7	8	9
72	1	2	3	4	5	6	7	8	9
73	1	2	3	4	5	6	7	8	9
74	1	2	3	4	5	6	7	8	9
75	1	2	3	4	5	6	7	8	9
76	1	2	3	4	5	6	7	8	9
77	1	2	3	4	5	6	7	8	9
78	1	2	3	4	5	6	7	8	9
79	1	2	3	4	5	6	7	8	9
80	1	2	3	4	5	6	7	8	9
81	1	2	3	4	5	6	7	8	9
82	1	2	3	4	5	6	7	8	9
83	1	2	3	4	5	6	7	8	9
84	1	2	3	4	5	6	7	8	9
85	1	2	3	4	5	6	7	8	9
86	1	2	3	4	5	6	7	8	9
87	1	2	3	4	5	6	7	8	9
88	1	2	3	4	5	6	7	8	9
89	1	2	3	4	5	6	7	8	9
90	1	2	3	4	5	6	7	8	9
91	1	2	3	4	5	6	7	8	9
92	1	2	3	4	5	6	7	8	9
93	1	2	3	4	5	6	7	8	9
94	1	2	3	4	5	6	7	8	9
95	1	2	3	4	5	6	7	8	9
96	1	2	3	4	5	6	7	8	9
97	1	2	3	4	5	6	7	8	9
98	1	2	3	4	5	6	7	8	9
99	1	2	3	4	5	6	7	8	9
100	1	2	3	4	5	6	7	8	9
101	1	2	3	4	5	6	7	8	9
102	1	2	3	4	5	6	7	8	9
103	1	2	3	4	5	6	7	8	9
104	1	2	3	4	5	6	7	8	9
105	1	2	3	4	5	6	7	8	9
106	1	2	3	4	5	6	7	8	9
107	1	2	3	4	5	6	7	8	9
108	1	2	3	4	5	6	7	8	9
109	1	2	3	4	5	6	7	8	9
110	1	2	3	4	5	6	7	8	9
111	1	2	3	4	5	6	7	8	9
112	1	2	3	4	5	6	7	8	9
113	1	2	3	4	5	6	7	8	9
114	1	2	3	4	5	6	7	8	9
115	1	2	3	4	5	6	7	8	9
116	1	2	3	4	5	6	7	8	9
117	1	2	3	4	5	6	7	8	9
118	1	2	3	4	5	6	7	8	9
119	1	2	3	4	5	6	7	8	9
120	1	2	3	4	5	6	7	8	9
121	1	2	3	4	5	6	7	8	9
122	1	2	3	4	5	6	7	8	9
123	1	2	3	4	5	6	7	8	9
124	1	2	3	4	5	6	7	8	9
125	1	2	3	4	5	6	7	8	9
126	1	2	3	4	5	6	7	8	9
127	1	2	3	4	5	6	7	8	9
128	1	2	3	4	5	6	7	8	9
129	1	2	3	4	5	6	7	8	9
130	1	2	3	4	5	6	7	8	9
131	1	2	3	4	5	6	7	8	9
132	1	2	3	4	5	6	7	8	9
133	1	2	3	4	5	6	7	8	9
134	1	2	3	4	5	6	7	8	9
135	1	2	3	4	5	6	7	8	9
136	1	2	3	4	5	6	7	8	9
137	1	2	3	4	5	6	7	8	9
138	1	2	3	4	5	6	7	8	9
139	1	2	3	4	5	6	7	8	9
140	1	2	3	4	5	6	7	8	9
141	1	2	3	4	5	6	7	8	9
142	1	2	3	4	5	6	7	8	9
143	1	2	3	4	5	6	7	8	9
144	1	2	3	4	5	6	7	8	9
145	1	2	3	4	5	6	7	8	9
146	1	2	3	4	5	6	7	8	9
147	1	2	3	4	5	6	7	8	9
148	1	2	3	4	5	6	7	8	9
149	1	2	3	4	5	6	7	8	9
150	1	2	3	4	5	6	7	8	9
151	1	2	3	4	5	6	7	8	9
152	1	2	3	4	5	6	7	8	9
153	1	2	3	4	5	6	7	8	9
154	1	2	3	4	5	6	7	8	9
155	1	2	3	4	5	6	7	8	9
156	1	2	3	4	5	6	7	8	9
157	1	2	3	4	5	6	7	8	9
158	1	2	3	4	5	6	7	8	9
159	1	2	3	4	5	6	7	8	9
160	1	2	3	4	5	6	7	8	9
161	1	2	3	4	5	6	7	8	9
162	1	2	3	4	5	6	7	8	9
163	1	2	3	4	5	6	7	8	9
164	1	2	3	4	5	6	7	8	9
165	1	2	3	4	5	6	7	8	9
166	1	2	3	4	5	6	7	8	9
167	1	2	3	4	5	6	7	8	9
168	1	2	3	4	5	6	7	8	9
169	1	2	3	4	5	6	7	8	9
170	1	2	3	4	5	6	7	8	9
171	1	2	3	4	5	6	7	8	9
172	1	2	3	4	5	6	7	8	9
173	1	2	3	4	5	6	7	8	9
174	1	2	3	4	5	6	7	8	9
175	1	2	3	4	5	6	7	8	9
176	1	2	3	4	5	6	7	8	9
177	1	2	3	4	5	6	7	8	9
178	1	2	3	4	5	6	7	8	9
179	1	2	3	4	5	6	7	8	9
180	1	2	3	4	5	6	7	8	9
181	1	2	3	4	5	6	7	8	9
182	1	2	3	4	5	6	7	8	9
183	1	2	3	4	5	6	7	8	9
184	1	2	3	4	5	6	7	8	9
185	1	2	3	4	5	6			

Subprocessor 5-B														
# active ft	0		12		12		16		24		12		24	
	12		20		24		24		24		24		24	
	24		24		24		24		24		24		24	
# buffers	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Configuration	40	80	120	160	240	240	240	240	240	240	240	240	240	240
FI_5A1	5A	1	1	1	1	1	1	1	1	1	1	1	1	1
FI_5A2	5A	2	2	2	2	2	2	2	2	2	2	2	2	2
FI_5A3	5A	17	17	17	17	17	17	17	17	17	17	17	17	17
FI_5B1	5B	3	3	3	3	3	3	3	3	3	3	3	3	3
FI_5B2	5B	4	4	4	4	4	4	4	4	4	4	4	4	4
FI_5B3	5B	19	19	19	19	19	19	19	19	19	19	19	19	19
FI_5C1	5C	5	5	5	5	5	5	5	5	5	5	5	5	5
FI_5C2	5C	6	6	6	6	6	6	6	6	6	6	6	6	6
FI_5C3	5C	21	21	21	21	21	21	21	21	21	21	21	21	21
FI_5D1	5D	7	7	7	7	7	7	7	7	7	7	7	7	7
FI_5D2	5D	8	8	8	8	8	8	8	8	8	8	8	8	8
FI_5D3	5D	23	23	23	23	23	23	23	23	23	23	23	23	23
FI_13A1	13A	9	9	9	9	9	9	9	9	9	9	9	9	9
FI_13A2	13A	10	10	10	10	10	10	10	10	10	10	10	10	10
FI_13B1	13B	11	11	11	11	11	11	11	11	11	11	11	11	11
FI_13B2	13B	12	12	12	12	12	12	12	12	12	12	12	12	12
FI_13C1	13C	13	13	13	13	13	13	13	13	13	13	13	13	13
FI_13C2	13C	14	14	14	14	14	14	14	14	14	14	14	14	14
FI_13D1	13D	15	15	15	15	15	15	15	15	15	15	15	15	15
FI_13D2	13D	16	16	16	16	16	16	16	16	16	16	16	16	16
FI_21A1	21A	17	17	17	17	17	17	17	17	17	17	17	17	17
FI_21A2	21A	18	18	18	18	18	18	18	18	18	18	18	18	18
FI_21B1	21B	19	19	19	19	19	19	19	19	19	19	19	19	19
FI_21B2	21B	20	20	20	20	20	20	20	20	20	20	20	20	20
FI_21C1	21C	21	21	21	21	21	21	21	21	21	21	21	21	21
FI_21C2	21C	22	22	22	22	22	22	22	22	22	22	22	22	22
FI_21D1	21D	23	23	23	23	23	23	23	23	23	23	23	23	23
FI_21D2	21D	24	24	24	24	24	24	24	24	24	24	24	24	24
FI_29A1	29A										2		2	2
FI_29B1	29B										4		4	4
FI_29C1	29C										6		6	6
FI_29D1	29D										8		8	8
FI_37A1	37A										10		10	10
FI_37B1	37B										12		12	12
FI_37C1	37C										14		14	14
FI_37D1	37D										16		16	16
FI_45A1	45A										18		18	18
FI_45B1	45B										20		20	20
FI_45C1	45C										22		22	22
FI_45D1	45D										24		24	24

40 total

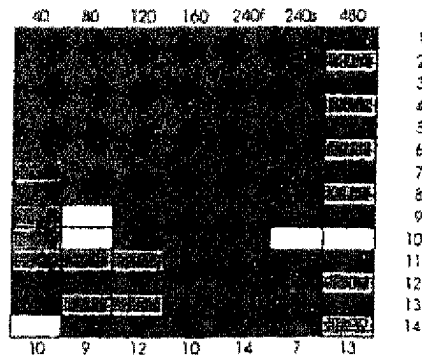


16 internal 1:2 fanout buffers  
12 internal 1:1 buffers (one output can be turned off)



Unstriper							
# active rx	10	9	12	10	14	7	13
# fabrics	1	2	3	4	6	6	12
Configuration	40	80	120	160	240f	240s	480
S_1A1	1	1	1	1	1	1	1
S_1A2	2	2	2	2	2		
S_1A3	11	11	11				
S_1A4	9						
S_1A5	7						
F1_1A1	3	3	3	3	3	3	3
F1_1A2	4	4	4	4	4		
F1_1A3	12	12	12				
F1_1A4	10						
F1_1A5	8						
F2_1A1	5	5	5	5	5	5	
F2_1A2	6	6	6	6			
F2_1A3	13	13					
F3_1A1	7	7	7	7	7		
F3_1A2	8	8	8				
F3_1A3	14						
F4_1A1	9	9	9	9			
F4_1A2	10	10					
F5_1A1	11	11	11				
F5_1A2	12						
F6_1A1	13	13	13				
F6_1A2	14						
F7_1A1					2		
F8_1A1					4		
F9_1A1					6		
F10_1A1					8		
F11_1A1					12		
F12_1A1					14		

Total 28



3 external 2:1 Mux's  
11 internal 2:1 Mux's  
3 internal 1:1 input buffers (one input can be disabled)

gfs ASIC Blockplane Connection Map

Revision	Date	Comments
1	11/3/99	First release, checked by Speiser
2	11/6/99	Changed AGG assignments for channels 7 and 9; corrects the sliper and unslipeir only
		Changed AGG 120G assignments for channels 17-24 to make Separator 1-4 and Separator 5-8 symmetric (Separator 5-8 is now a subset of Separator 1-4)
3	11/30/99	Corrected by Speiser and Benicsh Added control port assignments

Fabric to Blade egress bus format: <fabric> <blades> <channels> <slanes> <ports>
Fabric slot Blade slot Channel Lane Port
F1-F123 1-48 A-D 1-5 P-N

Noting convention:

Notes:

- 1) Map shown for a single instance of each ASIC, e.g. sliper channel A for blade number 1. From an ASIC point of view, cell that is significant in this sliper table is the fabric number and the lane number. The topology is the same for each subsequent channel (B-D) except slot (7-48).
- 2) Polarity is required to distinguish the two physical wires forming a differential pair. For each table entry (e.g., each logical signal) there are two physical connections. For example, logical signal F2\_1A3 is really comprised of F2\_1A3P and F2\_1A3N, which connect fabric 2 to blade 1, unslipeir 1, lane 3. Polarity is not shown in the connection maps to make them easier to read.
- 3) How to use this map: For a given configuration (e.g. with one fabric installed, read down AGG column). Read down the column to determine the source for data present on on sliper output bus. Each row represents a single sliper output bus.
- 4) XXXXXX = not used in this Configuration
- 5) To aid in PCB routing and reduce design complexity, there are only two unique connection assignments, the unslipeir and the Separator 1-4 maps. The sliper map is a subset of the unslipeir map. The separator 5-8 map, the aggregator 1-4 map, and the aggregator 5-8 map are all subsets of the separator 1-4 map.
- 6) Up to four control ports are supported (see maps for aggregator 9 and separator 9). If not all four control ports are needed, some control port channels can be deleted. For example, if only two 25Gbps control ports are needed, control port channels C and D can be deleted.

Configuration							Slipper Output bus
40	60	120	160	240f	240s	480	
S <sub>1A1</sub>	S <sub>1A1</sub>	S <sub>1A1</sub>	S <sub>1A1</sub>	S <sub>1A1</sub>	S <sub>1A1</sub>	S <sub>1A1</sub>	1
S <sub>1A2</sub>	S <sub>1A2</sub>	S <sub>1A2</sub>	S <sub>1A2</sub>			F7 <sub>1A1</sub>	2
F1 <sub>1A1</sub>	F1 <sub>1A1</sub>	F1 <sub>1A1</sub>	F1 <sub>1A1</sub>	F1 <sub>1A1</sub>	F1 <sub>1A1</sub>	F1 <sub>1A1</sub>	3
F1 <sub>1A2</sub>	F1 <sub>1A2</sub>	F1 <sub>1A2</sub>	F1 <sub>1A2</sub>			F8 <sub>1A1</sub>	4
	F2 <sub>1A1</sub>	F2 <sub>1A1</sub>	F2 <sub>1A1</sub>	F2 <sub>1A1</sub>	F2 <sub>1A1</sub>	F2 <sub>1A1</sub>	5
	F2 <sub>1A2</sub>	F2 <sub>1A2</sub>	F2 <sub>1A2</sub>			F9 <sub>1A1</sub>	6
		F3 <sub>1A1</sub>	F3 <sub>1A1</sub>	F3 <sub>1A1</sub>	F3 <sub>1A1</sub>	F3 <sub>1A1</sub>	7
		F3 <sub>1A2</sub>	F3 <sub>1A2</sub>			F10 <sub>1A1</sub>	8
			F4 <sub>1A1</sub>	F4 <sub>1A1</sub>	F4 <sub>1A1</sub>	F4 <sub>1A1</sub>	9
S <sub>1A4</sub>			F4 <sub>1A2</sub>				10
F1 <sub>1A4</sub>				F5 <sub>1A1</sub>	F5 <sub>1A1</sub>	F5 <sub>1A1</sub>	11
S <sub>1A3</sub>						F11 <sub>1A1</sub>	12
F1 <sub>1A3</sub>				F6 <sub>1A1</sub>	F6 <sub>1A1</sub>	F6 <sub>1A1</sub>	13
						F12 <sub>1A1</sub>	14

Aggregator 1-4									
Configuration									
40	80	120	160	240f	240s	480	Aggregator Input bus		
F1_1A1	F1_1A1	F1_1A1	F1_1A1	F1_1A1	F1_1A1	F1_1A1	1		
F1_1A2	F1_1A2	F1_1A2	F1_1A2			F1_25A1	2		
F1_1B1	F1_1B1	F1_1B1	F1_1B1	F1_1B1	F1_1B1	F1_1B1	3		
F1_1B2	F1_1B2	F1_1B2	F1_1B2			F1_25B1	4		
F1_1C1	F1_1C1	F1_1C1	F1_1C1	F1_1C1	F1_1C1	F1_1C1	5		
F1_1C2	F1_1C2	F1_1C2	F1_1C2			F1_25C1	6		
F1_1D1	F1_1D1	F1_1D1	F1_1D1	F1_1D1	F1_1D1	F1_1D1	7		
F1_1D2	F1_1D2	F1_1D2	F1_1D2			F1_25D1	8		
F1_1A4		F1_9A1	F1_9A1	F1_9A1	F1_9A1	F1_9A1	9		
		F1_9A2	F1_9A2			F1_33A1	10		
F1_1B4		F1_9B1	F1_9B1	F1_9B1	F1_9B1	F1_9B1	11		
		F1_9B2	F1_9B2			F1_33B1	12		
F1_1C4		F1_9C1	F1_9C1	F1_9C1	F1_9C1	F1_9C1	13		
		F1_9C2	F1_9C2			F1_33C1	14		
F1_1D4		F1_9D1	F1_9D1	F1_9D1	F1_9D1	F1_9D1	15		
		F1_9D2	F1_9D2			F1_33D1	16		
F1_1A3				F1_17A1	F1_17A1	F1_17A1	17		
						F1_41A1	18		
F1_1B3				F1_17B1	F1_17B1	F1_17B1	19		
						F1_41B1	20		
F1_1C3				F1_17C1	F1_17C1	F1_17C1	21		
						F1_41C1	22		
F1_1D3				F1_17D1	F1_17D1	F1_17D1	23		
						F1_41D1	24		



Configuration								Aggregator Input bus
40	80	120	160	240i	240s	480		
F1_CP_A1	F1_CP_A1	F1_CP_A1	F1_CP_A1	F1_CP_A1	F1_CP_A1	F1_CP_A1	1	
F1_CP_A2	F1_CP_A2	F1_CP_A2	F1_CP_A2				2	
F1_CP_B1	F1_CP_B1	F1_CP_B1	F1_CP_B1	F1_CP_B1	F1_CP_B1	F1_CP_B1	3	
F1_CP_D2	F1_CP_D2	F1_CP_D2	F1_CP_D2				4	
F1_CP_C1	F1_CP_C1	F1_CP_C1	F1_CP_C1	F1_CP_C1	F1_CP_C1	F1_CP_C1	5	
F1_CP_C2	F1_CP_C2	F1_CP_C2	F1_CP_C2				6	
F1_CP_D1	F1_CP_D1	F1_CP_D1	F1_CP_D1	F1_CP_D1	F1_CP_D1	F1_CP_D1	7	
F1_CP_D2	F1_CP_D2	F1_CP_D2	F1_CP_D2				8	
F1_CP_A4							9	
F1_CP_B4							10	
F1_CP_C4							11	
F1_CP_D4							12	
F1_CP_A3							13	
F1_CP_D3							14	
F1_CP_C3							15	
F1_CP_D3							16	
F1_CP_C3							17	
F1_CP_D3							18	
F1_CP_C3							19	
F1_CP_D3							20	
F1_CP_C3							21	
F1_CP_D3							22	
F1_CP_C3							23	
F1_CP_D3							24	

Separator 1-4							Separator Output Bus
Configuration							
40	80	120	160	240	240S	480	1
FI_1A1	FI_1A1	FI_1A1	FI_1A1	FI_1A1	FI_1A1	FI_1A1	FI_1A1
FI_1A2	FI_1A2	FI_1A2	FI_1A2	FI_1A2		FI_2BA1	2
FI_1B1	FI_1B1	FI_1B1	FI_1B1	FI_1B1	FI_1B1	FI_1B1	FI_1B1
FI_1B2	FI_1B2	FI_1B2	FI_1B2	FI_1B2		FI_2BA1	3
FI_1C1	FI_1C1	FI_1C1	FI_1C1	FI_1C1	FI_1C1	FI_1C1	FI_1C1
FI_1C2	FI_1C2	FI_1C2	FI_1C2	FI_1C2		FI_2BC1	4
FI_1D1	FI_1D1	FI_1D1	FI_1D1	FI_1D1	FI_1D1	FI_1D1	FI_1D1
FI_1D2	FI_1D2	FI_1D2	FI_1D2	FI_1D2		FI_2SD1	5
FI_1A4		FI_9A1	FI_9A1	FI_9A1	FI_9A1	FI_9A1	FI_9A1
FI_1A5		FI_9A2	FI_9A2	FI_9A2		FI_3SA1	6
FI_1B4		FI_9B1	FI_9B1	FI_9B1	FI_9B1	FI_9B1	FI_9B1
FI_1B5		FI_9B2	FI_9B2	FI_9B2		FI_3SB1	7
FI_1C4		FI_9C1	FI_9C1	FI_9C1	FI_9C1	FI_9C1	FI_9C1
FI_1C5		FI_9C2	FI_9C2	FI_9C2		FI_3SC1	8
FI_1D4		FI_9D1	FI_9D1	FI_9D1	FI_9D1	FI_9D1	FI_9D1
FI_1D5		FI_9D2	FI_9D2	FI_9D2		FI_3SD1	9
FI_1A3	FI_1A3	FI_1A3		FI_17A1	FI_17A1	FI_17A1	FI_17A1
FI_1B3	FI_1B3	FI_1B3		FI_17B1	FI_17B1	FI_17B1	FI_17B1
FI_1C3	FI_1C3	FI_1C3		FI_17C1	FI_17C1	FI_17C1	FI_17C1
FI_1D3	FI_1D3	FI_1D3		FI_17D1	FI_17D1	FI_17D1	FI_17D1
FI_1D3	FI_1D3	FI_1D3		FI_17D2		FI_17D1	FI_17D1
FI_1D3	FI_1D3	FI_1D3		FI_17D2		FI_17D1	FI_17D1
FI_1D3	FI_1D3	FI_1D3		FI_17D2		FI_17D1	FI_17D1
FI_1D3	FI_1D3	FI_1D3		FI_17D2		FI_17D1	FI_17D1
FI_1D3	FI_1D3	FI_1D3		FI_17D2		FI_17D1	FI_17D1
FI_1D3	FI_1D3	FI_1D3		FI_17D2		FI_17D1	FI_17D1
FI_1D3	FI_1D3	FI_1D3		FI_17D2		FI_17D1	FI_17D1
FI_1D3	FI_1D3	FI_1D3		FI_17D2		FI_17D1	FI_17D1
FI_1D3	FI_1D3	FI_1D3		FI_17D2		FI_17D1	FI_17D1
FI_1D3	FI_1D3	FI_1D3		FI_17D2		FI_17D1	FI_17D1
FI_1D3	FI_1D3	FI_1D3		FI_17D2		FI_17D1	FI_17D1
FI_1D3	FI_1D3	FI_1D3		FI_17D2		FI_17D1	FI_17D1
FI_1D3	FI_1D3	FI_1D3		FI_17D2		FI_17D1	FI_17D1
FI_1D3	FI_1D3	FI_1D3		FI_17D2		FI_17D1	FI_17D1
FI_1D3	FI_1D3	FI_1D3		FI_17D2		FI_17D1	FI_17D1
FI_1D3	FI_1D3	FI_1D3		FI_17D2		FI_17D1	FI_17D1
FI_1D3	FI_1D3	FI_1D3		FI_17D2		FI_17D1	FI_17D1
FI_1D3	FI_1D3	FI_1D3		FI_17D2		FI_17D1	FI_17D1
FI_1D3	FI_1D3	FI_1D3		FI_17D2		FI_17D1	FI_17D1
FI_1D3	FI_1D3	FI_1D3		FI_17D2		FI_17D1	FI_17D1
FI_1D3	FI_1D3	FI_1D3		FI_17D2		FI_17D1	FI_17D1
FI_1D3	FI_1D3	FI_1D3		FI_17D2		FI_17D1	FI_17D1
FI_1D3	FI_1D3	FI_1D3		FI_17D2		FI_17D1	FI_17D1
FI_1D3	FI_1D3	FI_1D3		FI_17D2		FI_17D1	FI_17D1
FI_1D3	FI_1D3	FI_1D3		FI_17D2		FI_17D1	FI_17D1
FI_1D3	FI_1D3	FI_1D3		FI_17D2		FI_17D1	FI_17D1
FI_1D3	FI_1D3	FI_1D3		FI_17D2		FI_17D1	FI_17D1
FI_1D3	FI_1D3	FI_1D3		FI_17D2		FI_17D1	FI_17D1
FI_1D3	FI_1D3	FI_1D3		FI_17D2		FI_17D1	FI_17D1
FI_1D3	FI_1D3	FI_1D3		FI_17D2		FI_17D1	FI_17D1
FI_1D3	FI_1D3	FI_1D3		FI_17D2		FI_17D1	FI_17D1
FI_1D3	FI_1D3	FI_1D3		FI_17D2		FI_17D1	FI_17D1
FI_1D3	FI_1D3	FI_1D3		FI_17D2		FI_17D1	FI_17D1
FI_1D3	FI_1D3	FI_1D3		FI_17D2		FI_17D1	FI_17D1
FI_1D3	FI_1D3	FI_1D3		FI_17D2		FI_17D1	FI_17D1
FI_1D3	FI_1D3	FI_1D3		FI_17D2		FI_17D1	FI_17D1
FI_1D3	FI_1D3	FI_1D3		FI_17D2		FI_17D1	FI_17D1
FI_1D3	FI_1D3	FI_1D3		FI_17D2		FI_17D1	FI_17D1
FI_1D3	FI_1D3	FI_1D3		FI_17D2		FI_17D1	FI_17D1
FI_1D3	FI_1D3	FI_1D3		FI_17D2		FI_17D1	FI_17D1
FI_1D3	FI_1D3	FI_1D3		FI_17D2		FI_17D1	FI_17D1
FI_1D3	FI_1D3	FI_1D3		FI_17D2		FI_17D1	FI_17D1
FI_1D3	FI_1D3	FI_1D3		FI_17D2		FI_17D1	FI_17D1
FI_1D3	FI_1D3	FI_1D3		FI_17D2		FI_17D1	FI_17D1
FI_1D3	FI_1D3	FI_1D3		FI_17D2		FI_17D1	FI_17D1
FI_1D3	FI_1D3	FI_1D3		FI_17D2		FI_17D1	FI_17D1
FI_1D3	FI_1D3	FI_1D3		FI_17D2		FI_17D1	FI_17D1
FI_1D3	FI_1D3	FI_1D3		FI_17D2		FI_17D1	FI_17D1
FI_1D3	FI_1D3	FI_1D3		FI_17D2		FI_17D1	FI_17D1
FI_1D3	FI_1D3	FI_1D3		FI_17D2		FI_17D1	FI_17D1
FI_1D3	FI_1D3	FI_1D3		FI_17D2		FI_17D1	FI_17D1
FI_1D3	FI_1D3	FI_1D3		FI_17D2		FI_17D1	FI_17D1
FI_1D3	FI_1D3	FI_1D3		FI_17D2		FI_17D1	FI_17D1
FI_1D3	FI_1D3	FI_1D3		FI_17D2		FI_17D1	FI_17D1
FI_1D3	FI_1D3	FI_1D3		FI_17D2		FI_17D1	FI_17D1
FI_1D3	FI_1D3	FI_1D3		FI_17D2		FI_17D1	FI_17D1
FI_1D3	FI_1D3	FI_1D3		FI_17D2		FI_17D1	FI_17D1
FI_1D3	FI_1D3	FI_1D3		FI_17D2		FI_17D1	FI_17D1
FI_1D3	FI_1D3	FI_1D3		FI_17D2		FI_17D1	FI_17D1
FI_1D3	FI_1D3	FI_1D3		FI_17D2		FI_17D1	FI_17D1
FI_1D3	FI_1D3	FI_1D3		FI_17D2		FI_17D1	FI_17D1
FI_1D3	FI_1D3	FI_1D3		FI_17D2		FI_17D1	FI_17D1
FI_1D3	FI_1D3	FI_1D3		FI_17D2		FI_17D1	FI_17D1
FI_1D3	FI_1D3	FI_1D3		FI_17D2		FI_17D1	FI_17D1
FI_1D3	FI_1D3	FI_1D3		FI_17D2		FI_17D1	FI_17D1
FI_1D3	FI_1D3	FI_1D3		FI_17D2		FI_17D1	FI_17D1
FI_1D3	FI_1D3	FI_1D3		FI_17D2		FI_17D1	FI_17D1
FI_1D3	FI_1D3	FI_1D3		FI_17D2		FI_17D1	FI_17D1
FI_1D3	FI_1D3	FI_1D3		FI_17D2		FI_17D1	FI_17D1
FI_1D3	FI_1D3	FI_1D3		FI_17D2		FI_17D1	FI_17D1
FI_1D3	FI_1D3	FI_1D3		FI_17D2		FI_17D1	FI_17D1
FI_1D3	FI_1D3	FI_1D3		FI_17D2		FI_17D1	FI_17D1
FI_1D3	FI_1D3	FI_1D3		FI_17D2		FI_17D1	FI_17D1
FI_1D3	FI_1D3	FI_1D3		FI_17D2		FI_17D1	FI_17D1
FI_1D3	FI_1D3	FI_1D3		FI_17D2		FI_17D1	FI_17D1
FI_1D3	FI_1D3	FI_1D3		FI_17D2		FI_17D1	FI_17D1
FI_1D3	FI_1D3	FI_1D3		FI_17D2		FI_17D1	FI_17D1
FI_1D3	FI_1D3	FI_1D3		FI_17D2		FI_17D1	FI_17D1
FI_1D3	FI_1D3	FI_1D3		FI_17D2		FI_17D1	FI_17D1
FI_1D3	FI_1D3	FI_1D3		FI_17D2		FI_17D1	FI_17D1
FI							

Separator 5-6

Configuration							Separator output bus
40	80	120	160	240	240s	480	
	F1_5A1	F1_5A1	F1_5A1	F1_5A1	F1_5A1	F1_5A1	1
	F1_5A2	F1_5A2	F1_5A2	F1_5A2		F1_29A1	2
	F1_5B1	F1_5B1	F1_5B1	F1_5B1	F1_5B1	F1_5B1	3
	F1_5B2	F1_5B2	F1_5B2	F1_5B2		F1_29B1	4
	F1_5C1	F1_5C1	F1_5C1	F1_5C1	F1_5C1	F1_5C1	5
	F1_5C2	F1_5C2	F1_5C2	F1_5C2		F1_29C1	6
	F1_5D1	F1_5D1	F1_5D1	F1_5D1	F1_5D1	F1_5D1	7
	F1_5D2	F1_5D2	F1_5D2	F1_5D2		F1_29D1	8
			F1_13A1	F1_13A1	F1_13A1	F1_13A1	9
			F1_13A2	F1_13A2		F1_37A1	10
			F1_13B1	F1_13B1	F1_13B1	F1_13B1	11
			F1_13B2	F1_13B2		F1_37B1	12
			F1_13C1	F1_13C1	F1_13C1	F1_13C1	13
			F1_13C2	F1_13C2		F1_37C1	14
			F1_13D1	F1_13D1	F1_13D1	F1_13D1	15
			F1_13D2	F1_13D2		F1_37D1	16
				F1_21A1	F1_21A1	F1_21A1	17
	F1_5A3	F1_5A3		F1_21A2		F1_45A1	18
	F1_5B3	F1_5B3		F1_21B1	F1_21B1	F1_21B1	19
				F1_21B2		F1_45B1	20
	F1_5C3	F1_5C3		F1_21C1	F1_21C1	F1_21C1	21
				F1_21C2		F1_45C1	22
	F1_5D3	F1_5D3		F1_21D1	F1_21D1	F1_21D1	23
				F1_21D2		F1_45D1	24



Configuration							Separator output bus
40	80	120	160	240	240s	480	
F1_CP_A1	F1_CP_A1	F1_CP_A1	F1_CP_A1	F1_CP_A1	F1_CP_A1	F1_CP_A1	1
F1_CP_A2	F1_CP_A2	F1_CP_A2	F1_CP_A2	F1_CP_A2			2
F1_CP_B1	F1_CP_B1	F1_CP_B1	F1_CP_B1	F1_CP_B1	F1_CP_B1	F1_CP_B1	3
F1_CP_B2	F1_CP_B2	F1_CP_B2	F1_CP_B2	F1_CP_B2			4
F1_CP_C1	F1_CP_C1	F1_CP_C1	F1_CP_C1	F1_CP_C1	F1_CP_C1	F1_CP_C1	5
F1_CP_C2	F1_CP_C2	F1_CP_C2	F1_CP_C2	F1_CP_C2			6
F1_CP_D1	F1_CP_D1	F1_CP_D1	F1_CP_D1	F1_CP_D1	F1_CP_D1	F1_CP_D1	7
F1_CP_D2	F1_CP_D2	F1_CP_D2	F1_CP_D2	F1_CP_D2			8
F1_CP_A4							9
F1_CP_A5							10
F1_CP_B4							11
F1_CP_B5							12
F1_CP_C4							13
F1_CP_C5							14
F1_CP_D4							15
F1_CP_D5							16
F1_CP_A3	F1_CP_A3	F1_CP_A3					17
F1_CP_B3	F1_CP_B3	F1_CP_B3					18
F1_CP_C3	F1_CP_C3	F1_CP_C3					19
F1_CP_D3	F1_CP_D3	F1_CP_D3					20
							21
							22
							23
							24

Configuration								Unstiffer Input bus
40	80	120	160	240	240s	480		
S_1A1	S_1A1	S_1A1	S_1A1	S_1A1	S_1A1	S_1A1	1	
S_1A2	S_1A2	S_1A2	S_1A2	S_1A2		F7_1A1	2	
F1_1A1	F1_1A1	F1_1A1	F1_1A1	F1_1A1	F1_1A1	F1_1A1	3	
F1_1A2	F1_1A2	F1_1A2	F1_1A2	F1_1A2		F0_1A1	4	
	F2_1A1	F2_1A1	F2_1A1	F2_1A1	F2_1A1	F2_1A1	5	
	F2_1A2	F2_1A2	F2_1A2	F2_1A2		F9_1A1	6	
S_1A5		F3_1A1	F3_1A1	F3_1A1	F3_1A1	F3_1A1	7	
F1_1A5		F3_1A2	F3_1A2	F3_1A2		F10_1A1	8	
S_1A6			F4_1A1	F4_1A1	F4_1A1	F4_1A1	9	
F1_1A4			F4_1A2				10	
S_1A3	S_1A1	S_1A3			F5_1A1	F0_1A1	11	
F1_1A3	F1_1A3	F1_1A3			F5_1A2	F11_1A1	12	
	F2_1A3	F2_1A3			F6_1A1	F0_1A1	13	
		F3_1A3			F6_1A2	F12_1A1	14	

**အိတ်စီအေအီးအေ**

ಮುಖ್ಯಮಂತ್ರಿ ಕುರಿತು  
 ಪುನಃ ರಾಜೀನಾಮೆ  
 ಸಲ್ಲಿಸಿದ ಬೆಳ್ಳೆ

45	60	125	160	210	240
1	1	2	4	5	0
2	6	3	3	2	2

```

c -- gpa/bits
c -- does not include spare
c -- number of 750MHz data bits from a fiber to egg/slug per OC-48 (3 per port card)

```

### Calculation

தமிழக அரசு

3.25	1.75	1.25	1	0.75	0.75
4	3	2	1	1	1

As bits per Tx  
round up to uni:

toxic to waterbirds

data on  
stability  
recovery

02	20	20	18	12	17
6.5	3.5	2.5	2	1.5	1.5
7	4	3	2	2	2

[illegible]

சென்னை, 14.05.2019

[illegible][illegible][illegible]

County:

100%	60%	1.20	186240	3407740	2.679489
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*modicus simplicioribus modica*

Page Card  
 2/1/2008  
 1/1/2008  
 1/1/2008

Active Tr  
Active Tr

10	3	10	12	7	13
2	2	14	4	4	11

max active Tx number of satellites per ship;  
max active Rx number of satellites per "master"  
number of satellites per port card

collected 3/10/87  
at 1000  
Washburn

THE UNIVERSITY OF CHICAGO

Year	1990	1991	1992	1993	1994	1995	1996	1997	1998	1999	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035	2036	2037	2038	2039	2040	2041	2042	2043	2044	2045	2046	2047	2048	2049	2050	2051	2052	2053	2054	2055	2056	2057	2058	2059	2060	2061	2062	2063	2064	2065	2066	2067	2068	2069	2070	2071	2072	2073	2074	2075	2076	2077	2078	2079	2080	2081	2082	2083	2084	2085	2086	2087	2088	2089	2090	2091	2092	2093	2094	2095	2096	2097	2098	2099	2100
1990	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100											

total. The number of gigabit backbones connections per subscriber number of gigabit backbones connections per subscriber.

Number of pol

FAVORIC  
Aug 1-4  
Aug 5-8  
Aug 9-4

മലിനം നിമ  
കലിനം നിമ  
കലിനം നിമ

18	16	16	20	12	2
3	3	16	29	12	2
20	24	24	24	24	2

most active in number of observations per odd group, but that active in number of observations per even group also included a smaller number of individuals that did separately.

பொருள் தருகின்ற  
தருகின்ற பொருள்

number of square footings per meter

485  
501  
515  
525

THE INSTITUTE  
FOR CREATION  
TEACHING

Year	1990	1991	1992	1993	1994	1995	1996	1997	1998	1999	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035	2036	2037	2038	2039	2040	2041	2042	2043	2044	2045	2046	2047	2048	2049	2050	2051	2052	2053	2054	2055	2056	2057	2058	2059	2060	2061	2062	2063	2064	2065	2066	2067	2068	2069	2070	2071	2072	2073	2074	2075	2076	2077	2078	2079	2080	2081	2082	2083	2084	2085	2086	2087	2088	2089	2090	2091	2092	2093	2094	2095	2096	2097	2098	2099	2100
1990	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100											

<b>total fix</b>	number of graphed backbones connecting per given egg group
<b>total fix</b>	number of graphed backbones per odd separator
<b>total fix</b>	number of graphed backbones per even separator

number of in-